Novel Architecture for Array and Radar Signal Processor (ARSP) for Active Phased Array Radars

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Abstract: - This paper presents a novel approach for combining digital beam former and Radar signal processor known as Array and Radar Signal Processor (ARSP) for multi-function active phased array radars. Signal processing and beam forming are the important functions of fully adaptive array radar. The proposed unit is capable of interacting with multiple (more than 144 numbers) digital receivers of Array Group Receivers (AGR) through high speed full duplex optical links. It is also interfaced with Radar Computing Unit (RCU) for dwell message reception and report transmission. This paper proposes the ARSP hardware configuration for rotating phased array radar. This hardware is configured to experiment the capabilities of adaptive beam forming and signal processing algorithms. The ARSP consists of optical to electrical conversion modules, the beam forming section followed by signal processing section. The paper also describes the functions of the various modules and configuration scheme for adaptive beam forming.

Keywords: DSP, ARSP, Beam forming, Optical tx/rx

INTRODUCTION

In most of the congenital radar systems the digital beam former (DBF) is built out of FPGAs and radar signal processor are made using high end processor as two different hardware units. This limits the capabilities of exploring advantages of using processors for recursive algorithms and floating point operations. Here these two units are combined together and a new architecture is proposed called Array and Radar Signal processor. The main functions of the proposed ARSP unit are Digital Beam Forming and the Programmable Signal Processing. Beam forming is a data intensive task in which samples from large number of array elements are combined to one or more output beams/channels through different arithmetic operations depending on the algorithms. Most of the beam forming algorithms is traditionally well suited for implementation in the FPGA and DSPs. ARSP unit is capable of receiving Digital I & Q data from multiple digital receivers (nearly 140) over 3.125Gbps full duplex optical Aurora links. The proposed hardware is cable of forming up to 24 multiple beams and signal processing on those multiple channels independently. The hardware is also capable of estimating the influence of jammer and hence best performance can be achieved in the jamming environment. Data logging facility is also provided for the purpose of debugging at different stages of ARSP, such that data can be selectively taped based on the requirement and can be send across 10GbE line to remotely located wide band recorder for offline analysis.

I. ARCHITECTURE

Existing equivalent hardware for the radars are bulkier and does not provide flexibility to include array signal processing and other advanced Radar signal processing scheme. The proposed ARSP hardware is a generic, flexible hardware solution that provides real time implementation of basic and advanced array and radar signal processing. The hardware envisages the use of state of art hardware units such as FPGAs, multi-core processors thereby achieving reduction in the hardware in terms of weight, volume, size and power consumption. It is also scalable and reconfigurable hardware architecture.

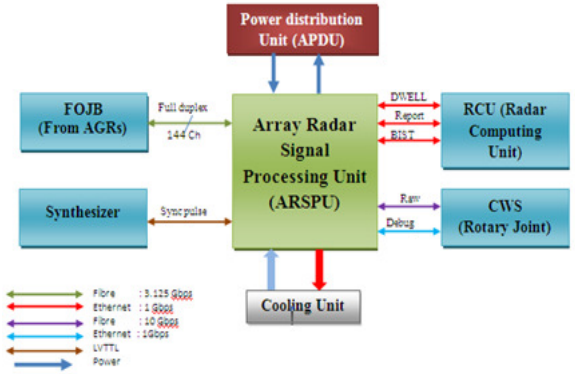

Figure 1: Interface Diagram

The figure-1 shows the external interface diagram of ARSP unit. It is interacting with multiple Array Group Receivers (AGRs), synthesizer, Radar Computing Unit (RCU) and Commander Work Station (CWS). ARSP

also acts as a communication interface between RCU and AGR to initialize, monitor AGR health, beam parameter transfer and for online calibration of antenna. This unit has three 1Gbps LAN and one 10Gbps LAN to full fill the other interfaces.

II. FUNCTIONAL REQUIREMENT

The proposed ARSP Unit will have following functional capabilities as shown in figure 2,

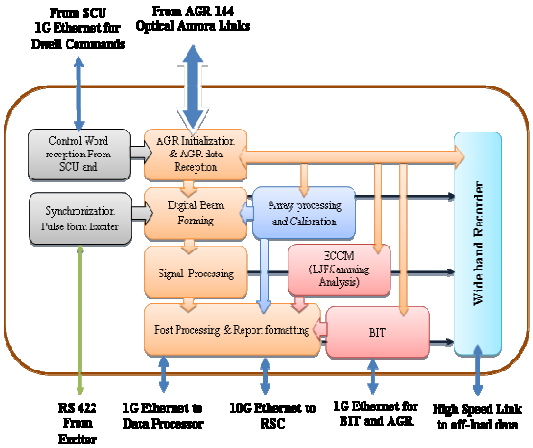

Figure 2: Functional flow diagram

a. Receive dwell parameters from RCU and distribute to all the AGRs and AGR initialization.
b. AGR data reception and synchronization.
c. Fixed and adaptive Digital Beam Forming i.e multiple beams on receive channels.
d. Programmable Signal Processing algorithms such as Digital Pulse Compression (DPC), FIR – FFT for pre-detection, CA/GO/SO/OS/TM/GM/Excision CFAR and Post detection processing.
e. ECCM (LJF calculation during Jamming Analysis).
f. Array processing and Calibration.
g. AGR data/ CFAR output Data recording capability.
h. BIT functionality.
i. Output of ARSP to RSC and RCU for further processing and presentation in the Display.

III. Hardware modules.

The proposed hardware architecture design is capable of meeting the interface, bandwidth and the functional requirements of the ARSP Unit., Customized FPGA based boards and the COTs CPU & GPGPU boards. The ARSP hardware configuration is shown in figure 3 and the unit consists of

1. Optical to Electrical converter
2. FPGA based Array Interface Boards
3. Processing FPGA Board
4. Multi core CPU
5. GPGPU board
6. Ethernet Switch Card

1. Optical to Electrical converter

Data capturing over two channel SFP module from each AGR is not a feasible solution as the number of AGRs increases. To optimize the size, power and volume we proposed VCSEL based optical to electrical transceiver, present technology allows us to receive up to 12 optical channels, and the size of module is less than an SFP module. So such 22 modules are used to achieve optical to electrical conversion and placed in a single PCB assembly from their high speed cable are used to distribute the data to array interface boards as electrical channels using high speed serial protocol.
Another optimized wireless solution we have proposed is to convert the optical to electrical conversion on the connector itself and the electrical lines to be distributed through backplane.

2. Array Interface board

Each Array Interface board (AIB) is capable of interfacing up to 40 complex video data from AGRs with in 6U VPX form factor and its major functions are listed below.

- Buffering of AGR data and synchronization
- De - multiplexing of the element data from AGR packet.
- Partial Beam formation of 40 AGR data to 24 (max) beams
- Packet formation and transmission of 24 channel partial beam data to Processing FPGA board for further processing
- Health status monitoring of AGRs and reporting it to central radar health monitoring system
- Transfer of dwell messages from radar computer to 40 AGRs
- Decimation of 5MHz AGR data to lower data rate for adaptive array signal processing.
- Data logging logic for Raw/Partial-beam data sending to the data recorder.

3. Processing FPGA board

The DBF algorithm is implemented in two stages. The first stage is performed in Array Interface card and the second stage in processing card. The Array interface card generates 24 partial beams. The partial beams from all Array interface cards are accumulated in processing card before sending for basic signal processing

operation. Other major functions of this card are listed bellow

- Glue logic between COTS hardware and FPGA Boards
- The pre-processing operation & pulse compression.

4. CPU and GPGPU board

The CPU COTs board will be used to perform the following operations:

- Collecting the CFAR output from the Processing FPGA Board (PFB)
- Post processing implementation
- CAL Processing
- Communication to RCU and RSC
- Master for GPGPU
- Master Controller for the system
- Interface to central BIT

The hardware consists of two octal-core Xeon processors on board.

The GPGPU COTS board will be used to perform the following operations:

- Advance processing for Adaptive Digital Beam Forming (ADBF) & Multi path mitigation
- Full Array signal processing operations
- Co-processor for CPU for high computational load

The FPGA based boards are custom designed as per the requirement. The CPU and GPGPU boards will be COTS hardware. All the boards are conduction cooled based on liquid cooling and will be integrated through a customized VPX high speed backplane. The total ARSP can be realized with eight slot solution by keeping one spare slots for future expansion.

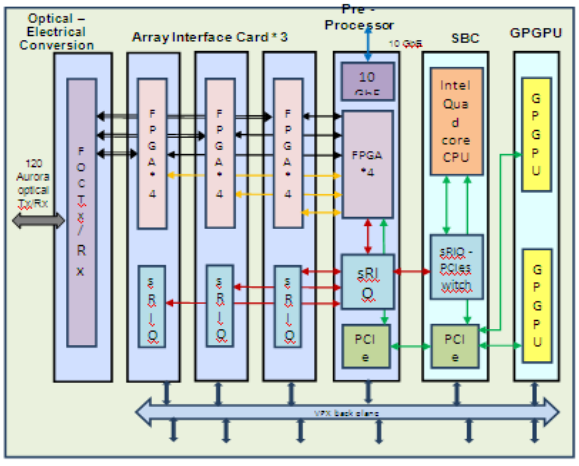

Fig3: HW Architecture

Realization approach

All the ARSP hardware boards are configured in 6U form factor in the VPX back plane. The ARSP configuration has 8 slots solutions by keeping the one spare slot for future expansion.

The total hardware solution will be capable of implementing Array Signal Processing and Radar Signal Processing along with the provision for recording the beam/raw data. The design is planned to provide three implementation options which are described as below.

Option 1: DBF & signal processing in FPGA and post processing in Intel CPU.

In this option, the interface boards receive data from the AGRs, perform the partial beam forming/ full beam forming for Full array/QG array configuration and send the data to the processing FPGA board. Weights for the beam-forming are pre-computed based on the beam requirements and are stored in the FPGAs. The processing FPGA board performs the final beam forming (in case of full array) and the fixed signal processing functions. The processed data is then sent to the Intel board for post processing. After post processing, the plots are sent to the radar computer.

For adaptive array processing and ECCM, the data from the AGRs are down sampled by the interface boards and are directly sent to the GPGPU board where the weight computation will be carried out and sent to the Array Interface Boards.

Option 2: DBF and Signal Processing in GPGPU.

In this option, the interface boards receive the data from the AGRs and will be send to processing FPGA board. The processing FPGA board synchronizes the data from the interface boards and sends it to the GPGPUs. The GPGPUs perform DBF and basic signal processing functions. The post processing is performed by the Intel CPU. The plots are then sent to the radar computer. However, due to the speed limits of the existing high speed links, this option is possible only for QG array configuration (Number of channels – 40).

Option 3: DBF in FPGA and complete Signal Processing in GPGPU.

In this option, the interface boards receives the data from the AGRs, performs partial DBF and sends the partial beams to the processing FPGA board where final beam forming is performed. The beam data is then sent to the GPGPUs where the basic and advanced signal processing functions including array signal processing are performed. The post processing is performed by the Intel CPU. The plots are then sent to the radar computer.

FPGA Resource and power Estimation

FPGA resources requirement calculation is done based on the logic simulations using ISE tool. The DBF and SP algorithms are implemented in floating point format. DSP Slices are used for implementing these floating point arithmetic blocks. Table 1 show the DSP slices requirement calculation for a digital Interface card, where the partial beam formations of 36 Sub Arrays are implemented.

	Per board (4 FPGA) DSP slice Utilization calculation for Digital Beam Formation	DSP slice Utilization
1	No. of Sub Arrays connected	36
2	DSP slices Requirement for single pair IQ, complex floating point multiplication	12
3	Complex. Mul section of 8 channels (8 Sub Arrays)	96
4	Combining of 8 channels	28
5	Partial Beam Formation of one Sub Array	124
6	Partial BF of 36 Sub Arrays	4464
7	Combining 36 channels	164
8	Beam formation for36 Sub Arrays	**4628**
9	**DSP slices Req. in the FPGA (200% of actual utilization)**	**9256**

Table1: DSP slice estimation for Array Interface Board

The FPGA power utilization is calculated using Xilinx Power estimator tool. For a single FPGA in digital Interface card 70% utilization is considered for DSP slices LUTs and Flip-Flops. 50% utilization is considered for Block RAMs. For the logic 250 MHz clock is considered on an average for a toggle rate of 12.5%. Ten numbers of 3.125 Gbps Aurora links are considered for a single FPGA. The total on-chip power is estimated to be 16.78W. Figure 5 shows the power estimation for a single FPGA in a Array Interface Board.

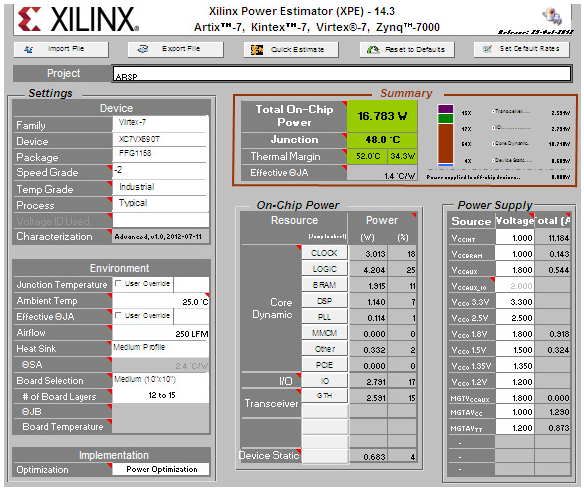

Fig5: On-chip power estimation for AIB FPGA

Conclusion

The future radars are going to be fully adaptive array with element level beam forming. The present hardware architecture is scalable with minimal hardware changes for the future requirements and can be used for interfacing with more number of AGR.

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